


# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

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Title of Invention	METHOD AND SYSTEM TO ENABLE AN ADAPTIVE LOAD BALANCING IN A PARALLEL PACKET SWITCH						
Application Number :	10/711320						
Confirmation Number:	5319						
First Named Applicant:	Rene Glaise						
Attorney Docket Number:	FR920030066US1						
Art Unit:	2661						
Examiner:							
Search string:	( 6824393 or 6728251 or 6667955 or 6661786 or 6606300 or 6584124 or 6522269 or 6452900 or 6424632 or 6421660 or 6411599 or 6370610 or 6343081 or 6324164 or 6317433 or 6189124 or 6125114 or 6108334 or 6101187 or 6097725 or 6055235 or 6014767 or 5818815 or 5761735 or 5694407 or 5539756 or 5459740 or 5359709 or 5043937 or 4961193 or 4712216 or 4931985 or 20040193997 or 20040143593 or 20040141510 or 20040141505 or 20040105384 or 20030182615 or 20020144208 or 20040136451 or 20040128094 or 20040103362 or 20030120992 or 20030118044 or 20030048787 or 20020182899 or 20020075871 or 20020024455 or 20020006110 or 20010036157 or 20030099250 or 20040141504 ).pn						
<b>US Patent Documents</b>							
<b>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</b>							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
/J.R./	1	6824393	2004-11-30	Debord, et al.			
/J.R./	2	6728251	2004-04-27	Blanc, et al.			
/J.R./	3	6667955	2003-12-23	Blanc, et al.			
/J.R./	4	6661786	2003-12-09	Abbate, et al.			
/J.R./	5	6606300	2003-08-12	Blanc, et al.			
/J.R./	6	6584124	2003-06-24	Blanc, et al.			
/J.R./	7	6522269	2003-02-18	Abbate, et al.			
/J.R./	8	6452900	2002-09-17	Blanc et al.			
/J.R./	9	6424632	2002-07-23	Poret, et al.			
/J.R./	10	6421660	2002-07-16	Glaise			
/J.R./	11	6411599	2002-06-25	Blanc, et al.			
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/J.R./	13	6343081	2002-01-29	Blanc, et al.			
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/J.R./	18	6108334	2000-08-22	Blanc, et al.			
/J.R./	19	6101187	2000-08-08	Cukier, et al.			
/J.R./	20	6097725	2000-08-01	Glaise, et al.			
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/J.R./	26	5539756	1996-07-23	Glaise, et al.			
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/J.R./	28	5359709	1994-10-25	Blanc, et al.			
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/J.R./	31	4712216	1987-12-08	Glaise			
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## US Published Applications

**Note: Applicant is not required to submit a paper copy of cited US Published Applications**

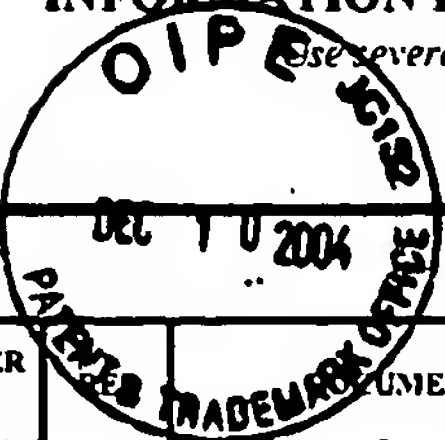
init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
/J.R./	1	20040193997	2004-09-30	Gallezot, et al.			
/J.R./	2	20040143593	2004-07-22	Le Maut, et al.			
/J.R./	3	20040141510	2004-07-22	Blanc, et al.			
/J.R./	4	20040141505	2004-07-22	Le Maut, et al.			
/J.R./	5	20040105384	2004-06-03	Gallezot, et. al.			
/J.R./	6	20030182615	2003-09-25	Gallezot, et al.			
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/J.R./	8	20040136451	2004-07-15	Blanc, et al.			
/J.R./	9	20040128094	2004-07-01	Blanc, et al.			
/J.R./	10	20040103362	2004-05-27	Glaise, et al.			
/J.R./	11	20030120992	2003-06-26	Glaise, et al.			
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/J.R./	14	20020182899	2002-12-05	Debord, et al.			
/J.R./	15	20020075871	2002-06-20	Blanc, et al.			
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/J.R./	20	20040141504	2004-07-22	Blanc, et al.			

## Signature

Examiner Name	Date
/Jeffrey Rutkowski/	10/25/2007

# INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)



Docket Number (Optional)

FR920030066US1

Application Number

10/711,320

Applicant(s)

Rene Glaise, et al.

Filing Date

09/10/2004

Group Art Unit

2661

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

/J.R./		Proc. ICC'92, 311.1.1-311.1.5, 1992, by T. ARAMAKI et al., 'PARALLEL "ATOM" SWITCH ARCHITECTURE FOR HIGH-SPEED ATM NETWORKS'

EXAMINER

/Jeffrey Rutkowski/

DATE CONSIDERED

10/25/2007

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.